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Set
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DB=PGPB, USPT, USOC; PLUR=YES; OP=OR

L1 (cache near5 coheren\$2 near5 memory) same (duplicat\$3 or copy) same (FIFO or buffer)

63 <u>L1</u>

Search Results -

Terms	Documents
(cache near5 coheren\$2 near5 memory) same (duplicat\$3 or copy) same (FIFO or buffer)	3

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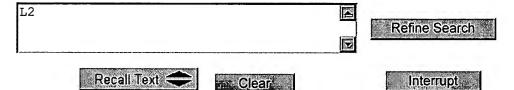
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DB=E	SPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
<u>L2</u>	(cache near5 coheren\$2 near5 memory) same (duplicat\$3 or copy) same (FIFO or buffer)	3	<u>L2</u>
DB=P	PGPB, USPT, USOC; PLUR=YES; OP=OR		
<u>L1</u>	(cache near5 coheren\$2 near5 memory) same (duplicat\$3 or copy) same (FIFO or buffer)	63	<u>L1</u>

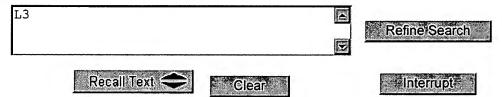
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DB=1	PGPB, USPT, USOC; PLUR=YES; OP=OR		
<u>L3</u>	710/306,312,112;711/141,148;709/213,214,253;370/401-402;707/201.ccls.	7242	<u>L3</u>
DB=I	EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
<u>L2</u>	(cache near5 coheren\$2 near5 memory) same (duplicat\$3 or copy) same (FIFO or buffer)	3	<u>L2</u>
DB=B	PGPB, USPT, USOC; PLUR=YES; OP=OR		
<u>L1</u>	(cache near5 coheren\$2 near5 memory) same (duplicat\$3 or copy) same (FIFO or buffer)	63	<u>L1</u>

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Terms	Documents
L1 and L3	16

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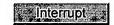
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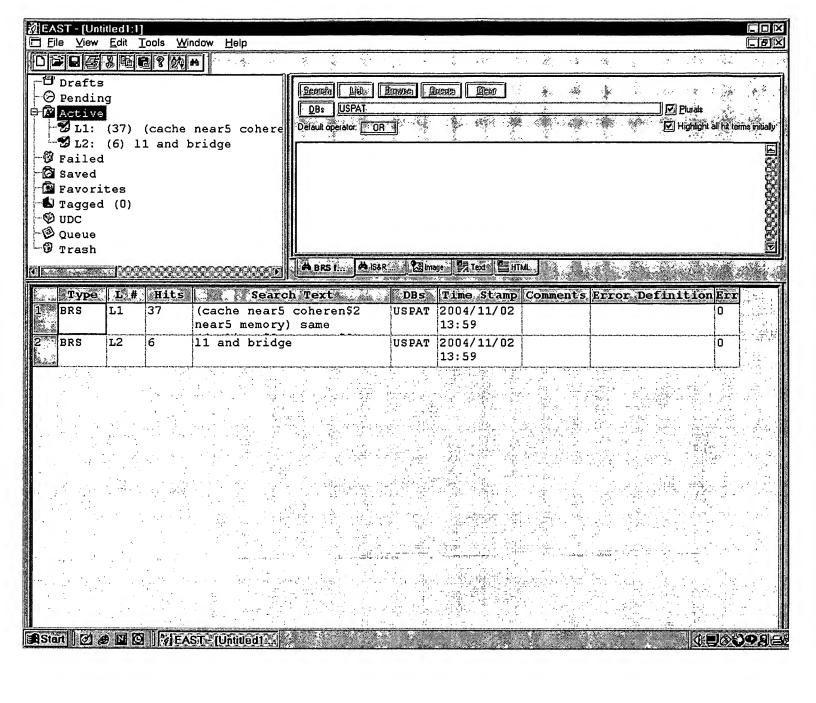


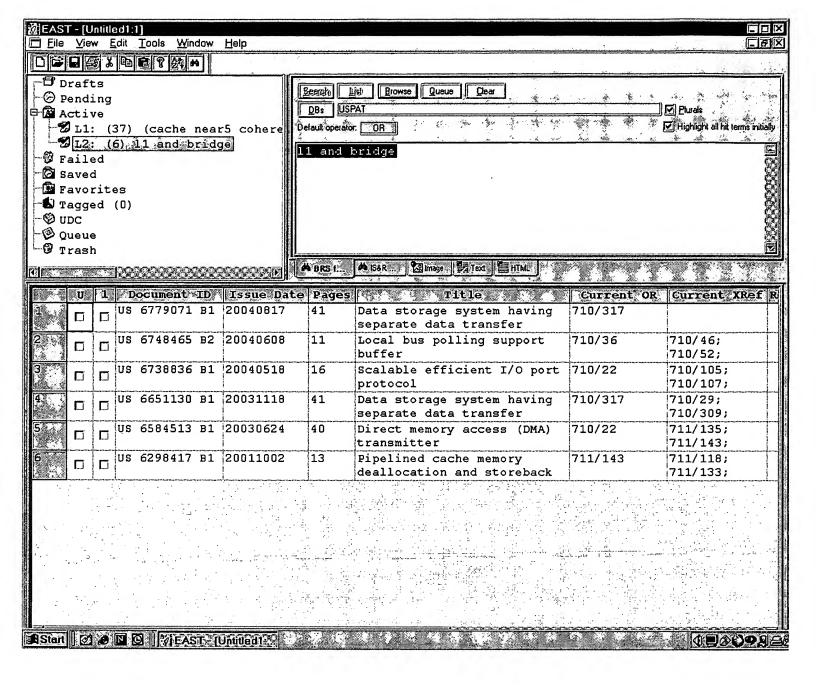


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DATE: Tuesday, November 02, 2004 Printable Copy Create Case

Set Name side by side	Query	<u>Hit</u> Count	<u>Set</u> <u>Name</u> result set
DB=B	PGPB, USPT, USOC; PLUR = YES; OP = OR		
<u>L4</u>	11 and L3	16	<u>L4</u>
<u>L3</u>	710/306,312,112;711/141,148;709/213,214,253;370/401-402;707/201.ccls.	7242	<u>L3</u>
DB=B	EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
<u>L2</u>	(cache near5 coheren\$2 near5 memory) same (duplicat\$3 or copy) same (FIFO or buffer)	3	<u>L2</u>
DB=I	PGPB, USPT, USOC; PLUR=YES; OP=OR		
<u>L1</u>	(cache near5 coheren\$2 near5 memory) same (duplicat\$3 or copy) same (FIFO or buffer)	63	<u>L1</u>





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Scalable Coherent Interface

Alnaes, K. Kristiansen, E.H. Gustavson, D.B. James, D.V.

Dolphin Server Technol. AS, Oslo, Norway;

This paper appears in: CompEuro '90. Proceedings of the 1990 IEEE Inte Conference on Computer Systems and Software Engineering

Meeting Date: 05/08/1990 - 05/10/1990

Publication Date: 8-10 May 1990

Location: Tel-Aviv Israel On page(s): 446 - 453 Reference Cited: 11

Inspec Accession Number: 3842745

Abstract:

The Scalable **Coherent** Interface Project (IEEE P1596) is establishing an interstandard for very-high-performance multiprocessors, supporting a **cache-cohemory** model scalable to systems with up to 64K nodes. The P1596 Scalable Interface (SCI) will supply a peak bandwidth per node of 1 Gb/s. The SCI star should facilitate assembly of processor, **memory**, I/O and bus **bridge** cards for multiple vendors into massively parallel systems with throughput far above we possible today. The SCI standard encompasses two levels of interface, a physical and a logical level. The physical level specifies electrical, mechanical and their characteristics of connectors and cards that meet the standard. The logical-level describes the address space, data transfer protocols, **cache coherence** mech synchronization primitives and error recovery. Logical-level issues such as parformats, packet transmission, transaction handshake, flow control, and **cache coherence** are addressed

Index Terms:

buffer storage computer interfaces multiprocessing systems standards 1 Gbit/s IE SCI standard Scalable Coherent Interface Project address space cache coherence mechanisms cache-coherent-memory model cards connectors data transfer prote electrical characteristics error recovery flow control interface standard logical level parallel systems mechanical characteristics packet formats packet transmission per bandwidth physical level synchronization primitives thermal characteristics transact handshake very-high-performance multiprocessors

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☐ 1. Document ID: NA9406319

Using default format because multiple data bases are involved.

L2: Entry 1 of 3

File: TDBD

Jun 1, 1994

TDB-ACC-NO: NA9406319

DISCLOSURE TITLE: Memory Queue Priority Mechanism for a RISC Processor

PUBLICATION-DATA:

IBM Technical Disclosure Bulletin, June 1994, US

VOLUME NUMBER: 37 ISSUE NUMBER: 6A

PAGE NUMBER: 319 - 322

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Full		Title	Citation	Front	Review	Classification	Date	Reference	Sauthus	Stachments.	Claims	KOMC	Draw, De
		2.	Docum	ent ID:	US 20	0030126341	l Al						
L	2:	Ent	rv 2 o:	f 3		F	ile:	DWPI			Jul 3	. 200	03

DERWENT-ACC-NO: 2003-688504

DERWENT-WEEK: 200365

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TITLE: Computer system with improved software to hardware communications has hardware device with cache memory that <u>duplicates</u> portion of <u>FIFO buffer</u> of main <u>memory array and that is kept coherent by way of cache coherency protocol</u>

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw

3. Document ID: WO 9003002 A, AU 8942117 A, AU 8944083 A, US 4928225 A, US 5029070 A

L2: Entry 3 of 3

File: DWPI

Mar 22, 1990

h eb b g ee ef e b ef b e

DERWENT-ACC-NO: 1990-116128

DERWENT-WEEK: 199015

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TITLE: Coherent cache structure method in multiprocessor system - ensure that most up-to-date copy is used without storing cache coherency status bits in global memory

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachme	rits Claims	KWIC	Dr
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☐ 1. Document ID: US 20030126341 A1

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L4: Entry 1 of 16

File: PGPB

Jul 3, 2003

PGPUB-DOCUMENT-NUMBER: 20030126341

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030126341 A1

TITLE: Method and apparatus for eliminating the software generated ready-signal to

hardware devices that are not part of the memory coherency domain

PUBLICATION-DATE: July 3, 2003

INVENTOR-INFORMATION:

NAME CITY STATE COUNTRY RULE-47

Bonola, Thomas J. Magnolia TX US
Larson, John E. Houston TX US
Olarig, Sompong P. Pleasonton CA US

US-CL-CURRENT: <u>710/306</u>

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWAC	Drawi D
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☐ 2. Document ID: US 20030033510 A1

L4: Entry 2 of 16 File: PGPB Feb 13, 2003

PGPUB-DOCUMENT-NUMBER: 20030033510

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030033510 A1

TITLE: Methods and apparatus for controlling speculative execution of instructions

based on a multiaccess memory condition

PUBLICATION-DATE: February 13, 2003

INVENTOR-INFORMATION:

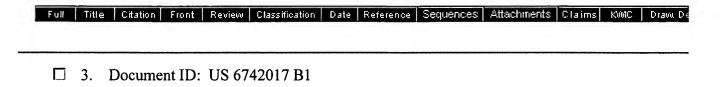
NAME CITY STATE COUNTRY RULE-47

Dice, David Foxborough MA US

US-CL-CURRENT: 712/235; 711/141

h eb b g e e e f b e

May 25, 2004



File: USPT

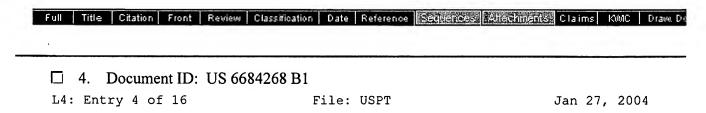
US-PAT-NO: 6742017

L4: Entry 3 of 16

DOCUMENT-IDENTIFIER: US 6742017 B1

TITLE: Data storage system having separate data transfer section and message

network with pointer or counters



US-PAT-NO: 6684268

DOCUMENT-IDENTIFIER: US 6684268 B1

TITLE: Data storage system having separate data transfer section and message network having CPU bus selector

Full	Title	Citation	Front	Review	Classification	Date	Reference	s(eleptorized)	Attachaenis:	Claims	KMC	Draw, De
	5.	Docume	nt ID:	US 66	47453 B1							
L4:	Ent	ry 5 of	£ 16		E	Tile:	USPT		1	Nov 11	. 200)3

US-PAT-NO: 6647453

DOCUMENT-IDENTIFIER: US 6647453 B1

TITLE: System and method for providing forward progress and avoiding starvation and livelock in a multiprocessor computer system

Full Title Citation Front Review Classifi	cation Date	Reference Sec	uences (Attachi	ients Claims	KWIC	Draw, De
☐ 6. Document ID: US 6631447	B1					
L4: Entry 6 of 16	File:	USPT		Oct 7,	200	3

US-PAT-NO: 6631447

DOCUMENT-IDENTIFIER: US 6631447 B1

TITLE: Multiprocessor system having controller for controlling the number of processors for which cache coherency must be guaranteed



h eb b g e e e f b ef b e

7. Document ID: US 6581112 B1

L4: Entry 7 of 16

File: USPT

Jun 17, 2003

US-PAT-NO: 6581112

DOCUMENT-IDENTIFIER: US 6581112 B1

TITLE: Direct memory access (DMA) receiver

Full Title Citation Front Review Classification Date Reference **Securences Attachments** Claims KMIC Draw De

□ 8. Document ID: US 6438659 B1

L4: Entry 8 of 16

File: USPT

Aug 20, 2002

US-PAT-NO: 6438659

DOCUMENT-IDENTIFIER: US 6438659 B1

TITLE: Directory based cache coherency system supporting multiple instruction

processor and input/output caches

Full Title Citation Front Review Classification Date Reference **Sequences Attachments** Claims KWIC Draw De

☐ 9. Document ID: US 6304932 B1

L4: Entry 9 of 16

File: USPT

Oct 16, 2001

US-PAT-NO: 6304932

DOCUMENT-IDENTIFIER: US 6304932 B1

TITLE: Queue-based predictive flow control mechanism with indirect determination of

queue fullness

Full Title Citation Front Review Classification Date Reference Sequences Attachments Claims KWC Draw De

☐ 10. Document ID: US 6182176 B1

L4: Entry 10 of 16

File: USPT

Jan 30, 2001

US-PAT-NO: 6182176

DOCUMENT-IDENTIFIER: US 6182176 B1

** See image for Certificate of Correction **

TITLE: Queue-based predictive flow control mechanism

h eb b g ee ef e b ef b e

Clear	Generate Collection	Print	Fwd Refs	Bkwd Refs	Generate OACS _a
F	Terms		Documents		
	L1 and L3				16

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☐ 11. Document ID: US 6122659 A

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L4: Entry 11 of 16

File: USPT

Sep 19, 2000

US-PAT-NO: 6122659

DOCUMENT-IDENTIFIER: US 6122659 A

TITLE: Memory controller for controlling memory accesses across networks in

distributed shared memory processing systems

DATE-ISSUED: September 19, 2000

INVENTOR-INFORMATION:

NAME CITY STATE ZIP CODE COUNTRY

Olnowich; Howard Thomas Endwell NY

US-CL-CURRENT: 709/213; 707/201, 709/214, 711/120

Full Title Citation Front Review Classification Date Reference Sequences Attachments Claims KWC Draw De

☐ 12. Document ID: US 6112283 A

L4: Entry 12 of 16

File: USPT

Aug 29, 2000

US-PAT-NO: 6112283

DOCUMENT-IDENTIFIER: US 6112283 A

TITLE: Out-of-order snooping for multiprocessor computer systems

Full Title Citation Front Review Classification Date Reference Sequences Attachifients Claims KMC Draw, De

☐ 13. Document ID: US 6044438 A

L4: Entry 13 of 16

File: USPT

Mar 28, 2000

US-PAT-NO: 6044438

DOCUMENT-IDENTIFIER: US 6044438 A

TITLE: Memory controller for controlling memory accesses across networks in

distributed shared memory processing systems

h e b b cg b cc e

Jun 25, 1996

Full Title Citation Front Review Classification Date Reference Sequences Attachments Claims KWC Draw De

14. Document ID: US 5960179 A

L4: Entry 14 of 16 File: USPT Sep 28, 1999

US-PAT-NO: 5960179

DOCUMENT-IDENTIFIER: US 5960179 A

** See image for Certificate of Correction **

TITLE: Method and apparatus extending coherence domain beyond a computer system bus

Full Title Citation Front Review Classification Date Reference Source des Alachmens Claims KWC Draw De

15. Document ID: US 5829033 A

L4: Entry 15 of 16 File: USPT Oct 27, 1998

US-PAT-NO: 5829033

DOCUMENT-IDENTIFIER: US 5829033 A

** See image for Certificate of Correction **

TITLE: Optimizing responses in a coherent distributed electronic system including a computer system

Full Title Citation Front Review Classification Date Reference Sequences Alignments Claims NMC Draw De

File: USPT

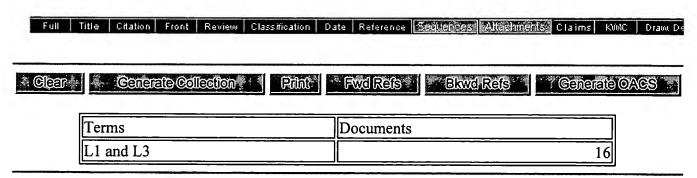
L4: Entry 16 of 16

US-PAT-NO: 5530933

DOCUMENT-IDENTIFIER: US 5530933 A

TITLE: Multiprocessor system for maintaining cache coherency by checking the

coherency in the order of the transactions being issued on the bus



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US-PAT-NO:

6298417

DOCUMENT-IDENTIFIER:

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US 6298417 B1

See image for Certificate of Correction

TITLE:

Pipelined cache memory deallocation and storeback

Previous patent

Detailed Description Text - DETX (5):

Computer system 100 typically further includes a first peripheral bus 110 connected to a peripheral port of bus interface unit 104. First peripheral bus 110 is suitably designed in accordance with an industry standard protocol such as the PCI, ISA, or EISA bus protocols to connect with peripheral devices such as peripheral device 120. Peripheral device 120 may comprise, in suitable embodiments, a hard disk controller, a CD controller, a video controller, a graphics accelerator, or various other peripheral devices. A bus <u>bridge</u> 122 provides a path between first peripheral bus 110 and a second peripheral bus 124. A second peripheral bus is frequently incorporated into a computer system 100 to increase the flexibility of computer system 100. In one common arrangement, first peripheral bus 110 complies with the PCI protocol while second bus 124 complies with the ISA standard such that computer system 100 maybe coupled to both PCI and ISA devices.

Detailed Description Text - DETX (9):

A cache miss occurs when processing unit 102 issues an instruction with a system memory address that is not currently reproduced in cache memory subsystem 106. When a miss corresponds to a modified cache, it is necessary to copy the data stored in the cache line to system memory 108 prior to re-writing the cache line with the information required by the cache miss cycle. The copyback process may unnecessarily and undesirably hamper system performance by consuming multiple clock cycles, especially if the cache line size is large relative to cache bus 203. Despite some disadvantages that accompany them, large cache lines are frequently preferred when implementing cache memory arrays to reduce the amount of circuitry required to implement cache tag RAM 206. A copyback of a modified cache line is typically accomplished by copying the line to a buffer or temporary storage location referred to for purposes of this disclosure as a storeback buffer. Accordingly, a preferred embodiment of

